



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,093	01/03/2001	Derrick I. Hisatake	10559-371001/P10177	4131

20985 7590 11/17/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER

ROCHE, TRENTON J

ART UNIT PAPER NUMBER

2124

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

56

Office Action Summary	Application No. 09/754,093	Applicant(s) HISATAKE, DERRICK I. JK	
	Examiner Trent J Roche	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 August 2004.
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6,8-15,17-22,24-29 and 31 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 1-6,8-15,17-22,24-29 and 31 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☒ The drawing(s) filed on 03 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2124

DETAILED ACTION

1. This office action is responsive to communications filed 27 August 2004.
2. Per applicant's request, amended claims 1, 9, 18 and 25 have been entered. Newly added claim 31 has been entered. Claims 1-6, 8-15, 17-22 and 24-29 and 31 are pending.
3. Claims 1-6, 8-15, 17-22 and 24-29 and 31 have been examined.

Response to Arguments

4. Applicant's remarks, filed 27 August 2004, have been fully considered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 18 recites the limitation "the flash erase" in line 6. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination this will be interpreted to read "the flash erase file."

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2124

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-6, 9-15, 18-22, 25-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,055,632 to Deegan et al in view of U.S. Patent 6,070,012 to Eitner et al.

Regarding claim 1:

Deegan et al teach:

- receiving, at a network device, an upgrade package (“receiving the firmware upgrade at a communication daughterboard of the programmable controller system...” in col. 3 lines 22-24)
- over a computer network sent from a client device, the upgrade package including upgrade software (“transferring the firmware to the non-volatile memory of the programmable controller system by way of the remote network connection.” in col. 3 lines 3-5)
- automatically upgrading internal software of a peripheral device installed in the network device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28. Further, the process occurs automatically, “the processor module could determine on its own that new firmware is required...” in col. 6 lines 62-63)
- a packet header, the packet header containing instructions for the peripheral device for overwriting contents of software in the peripheral device, and by transferring the packet

Art Unit: 2124

header and the upgrade software to the peripheral device by a connection (“transferring the firmware to the non-volatile memory of the programmable controller system by way of the remote network connection.” in col. 3 lines 3-5. A packet header is inherently part of the download package, as a packet header is part of any network communication.)

substantially as claimed. Deegan et al do not explicitly disclose the upgrade package including a flash erase file, and appending content of the flash erase file to a packet header. Eitner et al discloses in an analogous software upgrading system the aspects of appending a flash erase file to a packet header for transferring across a connection as claimed (“downloadable image includes...peripheral system download (PSDL) module which controls the actual erasing and burning of target packs in flash memory” in col. 6 line 65 to col. 7 line 2) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing and burning technique of Eitner et al with the firmware upgrading system of Deegan et al, as this would be one of the “conventional non-volatile memory programming techniques” for burning firmware, which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Deegan et al teach recognizing the received package as an upgrade based on information contained in the upgrade package (“the processor module must eventually...enter the special firmware upgrade mode...” in col. 7 lines 9-10. The fact that the system enters an upgrade mode means that the system has inherently recognized that the downloaded program is an upgrade, based on the contents of the file.)

Regarding claim 3:

Art Unit: 2124

The rejection of claim 1 is incorporated, and further, Deegan et al teach recognizing the received package as an upgrade package based on a filename extension associated with the package (Note rejection regarding claim 2. For the system to enter an upgrade mode, it must recognize the file as an upgrade, therefore inherently recognizes the file by checking the filename.)

Regarding claim 4:

The rejection of claim 1 is incorporated, and further, Deegan et al teach upgrading the internal software as claimed (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28.)

Regarding claim 5:

The rejection of claim 4 is incorporated, and further, Deegan et al teach upgrading the peripheral device as claimed (“enter the special firmware upgrade mode...” in col. 7 line 10. Further, the contents of the upgrade package are parsed into a format suitable for the device, as shown in col. 8 lines 22-36)

Regarding claim 6:

The rejection of claim 5 is incorporated, and further, Deegan et al teach issuing a command to the peripheral device as claimed (“enter the special firmware upgrade mode...” in col. 7 line 10. For the system to have entered an upgrade mode, it must have inherently received a command from the host computer notifying the device of an available upgrade.)

Art Unit: 2124

Regarding claim 9:

Deegan et al teach:

- a system comprising a computer network, a network device coupled to the network, a peripheral device installed within the network device; wherein the network device comprises a processor configured to receive over the network an upgrade package that includes upgrade software to update the peripheral device (Note Fig. 1 and 2, and further, “transferring the firmware to the non-volatile memory of the programmable controller system by way of the remote network connection.” in col. 3 lines 3-5)
- the packet header containing instructions for the peripheral device to overwrite contents of software in the peripheral device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28)
- transfer the packet header and the upgrade software to the peripheral device by a connection to automatically upgrade the peripheral device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28. Further, the process occurs automatically, “the processor module could determine on its own that new firmware is required...” in col. 6 lines 62-63)

substantially as claimed. Deegan et al do not explicitly disclose the upgrade package including a flash erase file, and appending content of the flash erase file to a packet header. Eitner et al discloses in an analogous software upgrading system the aspects of appending a flash erase file to a packet header for transferring across a connection as claimed (“downloadable image includes...peripheral system download (PSDL) module which controls the actual erasing and burning of target packs in flash

Art Unit: 2124

memory” in col. 6 line 65 to col. 7 line 2) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing and burning technique of Eitner et al with the firmware upgrading system of Deegan et al, as this would be one of the “conventional non-volatile memory programming techniques” for burning firmware, which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claim 10:

The rejection of claim 9 is incorporated, and further, Deegan et al teach a processor as claimed (Note Fig. 1 item 22, the microprocessor is installed on the remote device, which controls the upgrading of the firmware once it is downloaded to the system.)

Regarding claims 11-13:

The rejection of claim 9 is incorporated, and further, claims 11-13 are rejected for the reasons set forth in connection with claims 2-4, respectively.

Regarding claim 14:

The rejection of claim 13 is incorporated, and further, claim 14 is rejected for the reasons set forth in connection with claim 5.

Regarding claims 15:

The rejection of claim 14 is incorporated, and further, claims 15 is rejected for the reasons set forth in connection with claim 6.

Art Unit: 2124

Regarding claim 18:

Deegan et al teach:

- a computer-readable medium that stores computer-executable instructions (“a computer system...and...a plurality of programmable controller modules...” in col. 11 lines 64-66)
- recognize a received package as an upgrade package intended for a peripheral device installed in a network device, the upgrade package including upgrade software (“the processor module must eventually...enter the special firmware upgrade mode...” in col. 7 lines 9-10.
The fact that the system enters an upgrade mode means that the system has inherently recognized that the downloaded program is an upgrade.)
- the packet header containing instructions for the peripheral device to overwrite contents of software in the peripheral device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28)
- transfer the packet header and the upgrade software to the peripheral device by a connection to automatically upgrade internal software in the peripheral device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28. Further, the process occurs automatically, “the processor module could determine on its own that new firmware is required...” in col. 6 lines 62-63)

substantially as claimed. Deegan et al do not explicitly disclose the upgrade package including a flash erase file, and appending content of the flash erase file to a packet header. Eitner et al discloses in an analogous software upgrading system the aspects of appending a flash erase file to a packet header for transferring across a connection as claimed (“downloadable image includes...peripheral system

Art Unit: 2124

download (PSDL) module which controls the actual erasing and burning of target packs in flash memory” in col. 6 line 65 to col. 7 line 2) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing and burning technique of Eitner et al with the firmware upgrading system of Deegan et al, as this would be one of the “conventional non-volatile memory programming techniques” for burning firmware, which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claims 19 and 20:

The rejection of claim 18 is incorporated, and further, claims 19 and 20 are rejected for the reasons set forth in connection with claims 2 and 4, respectively.

Regarding claim 21:

The rejection of claim 20 is incorporated, and further, claim 21 is rejected for the reasons set forth in connection with claim 5.

Regarding claims 22:

The rejection of claim 21 is incorporated, and further, claims 22 is rejected for the reasons set forth in connection with claim 6.

Regarding claim 25:

Deegan et al teach:

- a port for coupling the apparatus to a network, a peripheral device installed in the apparatus, a processor (Note Fig. 1 and the corresponding section of the disclosure)

Art Unit: 2124

- the processor is configured to receive an upgrade package through the port, the upgrade package including upgrade software (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28)
- the packet header containing instructions for the peripheral device to overwrite contents of software in the peripheral device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28)
- transfer the packet header and the upgrade software to the peripheral device by a connection to automatically upgrade internal software in the peripheral device (“the firmware provider establishes a remote Ethernet link directly with the communication daughterboard, e.g., over the internet, and it is the firmware provider that conducts the firmware upgrade.” in col. 6 lines 24-28. Further, the process occurs automatically, “the processor module could determine on its own that new firmware is required...” in col. 6 lines 62-63)

substantially as claimed. Deegan et al do not explicitly disclose the upgrade package including a flash erase file, and appending content of the flash erase file to a packet header. Eitner et al discloses in an analogous software upgrading system the aspects of appending a flash erase file to a packet header for transferring across a connection as claimed (“downloadable image includes...peripheral system download (PSDL) module which controls the actual erasing and burning of target packs in flash memory” in col. 6 line 65 to col. 7 line 2) It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory erasing and burning technique of Eitner et al with the firmware upgrading system of Deegan et al, as this would be one of the “conventional

Art Unit: 2124

non-volatile memory programming techniques” for burning firmware, which Deegan et al indicates may be used, as shown in col. 8 lines 50-53 of Deegan et al.

Regarding claim 26:

The rejection of claim 25 is incorporated, and further, claim 25 is rejected for the reasons set forth in connection with claim 2.

Regarding claim 27:

The rejection of claim 26 is incorporated, and further, claim 27 is rejected for the reasons set forth in connection with claim 3.

Regarding claim 28:

The rejection of claim 25 is incorporated, and further, claim 28 is rejected for the reasons set forth in connection with claim 5.

Regarding claims 29:

The rejection of claim 28 is incorporated, and further, claim 29 is rejected for the reasons set forth in connection with claims 6.

Regarding claim 31:

The rejection of claim 1 is incorporated, and further, Deegan et al discloses the upgrading of the internal software of the peripheral device occurring independently of a particular type of operating system on the client device as claimed (“since there is no operating system during the firmware

Art Unit: 2124

upgrade...” in col. 7 lines 65-66. As there is no OS present during the upgrade, the upgrade is inherently independent of a particular type of operating system.)

10. Claims 8, 17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,055,632 to Deegan et al, in view of U.S. Patent 6,070,012 to Eitner et al, further in view of U.S. Patent 6,601,212 to Guha et al.

Regarding claim 8:

The rejection of claim 1 is incorporated, and further, neither Deegan et al nor Eitner et al teach sending a message indicating success or failure of the upgrade as claimed. Guha et al disclose in an analogous firmware upgrading system sending a message indicating success or failure to the client computer (“If an error is found, an error message will be sent to the client computer...if an error is not found, the peripheral device sends a download successful message to the client computer...” in col. 4 lines 16-30). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to implement the message indication capabilities of Guha et al in the firmware upgrading system of Deegan et al modified by Eitner et al, implemented via the addition of instructional code to transmit messages, as this would ensure that the upgrade is completed successfully by enabling the host computer to attempt to resend the upgrade if a failed upgrade message is received in the system disclosed by Deegan et al modified by Eitner et al.

Regarding claims 17 and 24:

Claims 17 and 24 recite a system and article for performing the method of claim 8, and are rejected for the reasons set forth in connection with claim 8.

Art Unit: 2124

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.



Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (571)272-3733. The examiner can normally be reached on Monday - Friday, 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trent J Roche
Examiner
Art Unit 2124

TJR

 
KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100